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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,700	09/29/2000	Daryl D. Starr	ALA-010B	9585

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EXAMINER	
BURGESS, BARBARA N	

ART UNIT	PAPER NUMBER
2157	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/675,700	STARR ET AL.	
	Examiner	Art Unit	
	Barbara N Burgess	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-4, 6-13, 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Muller et al. (hereinafter "Muller", 6,650,640 B1).

As per claim 1, Muller discloses an interface device connectable to a network, a computer and storage unit, the interface device comprising:

- A sequencer including a hardware logic circuit configured to process a transport layer header of a network packet (column 4, lines 48-50, column 7, lines 20-25, 31-35, 64-67, column 8, lines 1-5, 17-20, 50-60, column 9, lines 1-5, column 15, lines 35-38, column 35, lines 53-67, column 36, lines 11-30);
- A memory adapted to store control information regarding a network connection being handled by said device (column 4, lines 20-25, column 9, lines 14-16, 20-25, 56-58, column 10, lines 1-7, column 11, lines 46-59, column 12, lines 11-15, column 52, lines 64-67, column 53, lines 1-7);

- A mechanism for associating said packet with said control information and for selecting whether to process said packet by said computer or to send data from said packet to the storage unit, thereby avoiding the computer (column 4, lines 45-50, 58-67, column 8, lines 50-60, 66-67, column 9, lines 13-17, 22-35, 66-67, column 10, lines 2-7, column 11, lines 46-59, column 12, lines 11-15, column 16, lines 59-67).

As per claim 3, Muller discloses the interface device of claim 1, further comprising a plurality of network ports, wherein one of the said network ports is connectable to the storage unit (column 4, lines 40-43, column 6, lines 37-40, column 7, lines 15-19, column 8, lines 40-43, column 9, lines 1-5, column 10, lines 65-67).

As per claim 6, Muller discloses the network interface device of claim 1, further comprising a file cache adapted to store said data (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

As per claim 4, Muller discloses the interface device of claim 1, further comprising a Fibre Channel controller connectable to the storage unit (column 61, lines 55-60).

As per claim 7, Muller further discloses the network interface device of claim 1, further comprising a file cache adapted to store said data under control of a file system in the host (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

As per claim 8, Muller discloses an interface device, connectable to a network, to a storage unit and to a host having a CPU running a file system and a protocol processing stack, the interface device comprising:

- A memory having first and second portions, said first portion adapted to store a communication control block defining a network message that includes a plurality of packets containing data and control information, and said second portion adapted to cache file blocks that are stored on said storage unit, said communication control block indicating a source location and a destination location for said message such that one of said source and destination locations is disposed in said second portion of said memory, and the other of said source and destination locations is disposed on the network (column 4, lines 20-25, column 7, lines 20-45, column 9, lines 14-25, 56-58, column 10, lines 1-7, column 11, lines 46-59, column 12, lines 11-15, column 52, lines 64-67, column 53, lines 1-7);
- Circuitry adapted to categorize headers of said packets (column 4, lines 48-50, column 7, lines 20-25, 31-35, 64-67, column 8, lines 1-5, 17-20, 50-60, column 9, lines 1-5, column 15, lines 35-38, column 35, lines 53-67, column 36, lines 11-30);
- A processor adapted to associate said packets with said communication control block for sending said data to said destination without processing by the CPU (column 4, lines 45-50, 58-67, column 8, lines 50-60, 66-67, column 9, lines 13-17, 22-35, 66-67, column 10, lines 2-7, column 11, lines 46-59, column 12, lines 11-15, column 16, lines 59-67).

As per claim 9, Muller discloses the interface device of claim 8, wherein said communication control block is created by the protocol-processing stack (column 6, lines 62-67, column 7, lines 57-63, column 8, lines 9-20, column 9, lines 43-47, column 10, lines 50-65).

As per claim 10, Muller discloses the interface device of claim 8, wherein said second portion of said memory is managed by the file system (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52).

As per claim 11, Muller discloses the interface device of claim 8, wherein said circuitry is adapted to process a transport layer header of said headers (column 4, lines 48-50, column 7, lines 20-25, 31-35, 64-67, column 8, lines 1-5, 17-20, 50-60, column 9, lines 1-5, column 15, lines 35-38, column 35, lines 53-67, column 36, lines 11-30).

As per claim 12, Muller discloses the interface device of claim 8, wherein said circuitry is adapted to create a summary of at least one said packets to compare with said communication control block (column 4, lines 45-50, 58-67, column 8, lines 50-60, 66-67, column 9, lines 13-17, 22-35, 66-67, column 10, lines 2-7, column 11, lines 46-59, column 12, lines 11-15, column 16, lines 59-67).

As per claim 13, Muller discloses the interface device of claim 8, wherein said processor is configured to associate at least one of said packets with said communication control block by creating a header for said packet that is based on said communication control block and adding said header to said packet (column 9, lines 20-35, column 11, lines 46-60).

As per claim 15, discloses the interface device of claim 8, further comprising a network port adapted to connect with the storage unit (column 4, lines 40-43, column 6, lines 37-40, column 7, lines 15-19, column 8, lines 40-43, column 9, lines 1-5, column 10, lines 65-67).

As per claim 16, Muller discloses an interface device connectable to a local computer, a network and storage unit, the local computer having a CPU and a protocol processing stack, the interface device comprising:

- A memory including a file cache for temporary storage of data being transferred between the network and the storage unit (column 56, lines 20-30, column 58, lines 26-30, column 61, lines 34-35, column 62, lines 47-52);
- Slow-path means for processing a first packet of a message by sending the packet to the local computer for processing by the CPU running the protocol stack (column 6, lines 62-67, column 7, lines 57-63, column 8, lines 9-20, column 9, lines 43-47, column 10, lines 50-65);

- Fast-path means for transferring a second packet of said message between the network and the storage unit without processing by the CPU (column 4, lines 45-50, 58-67, column 8, lines 50-60, 66-67, column 9, lines 13-17, 22-35, 66-67, column 10, lines 2-7, column 11, lines 46-59, column 12, lines 11-15, column 16, lines 59-67).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 5, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (hereinafter "Muller", 6,650,640 B1) in view of Day et al. (hereinafter "Day", 6,065,096).

As per claim 2, Muller discloses the interface device of claim 1.

Muller does not explicitly disclose the interface further comprising a SCSI controller connectable to the storage unit.

However, Day discloses SCSI interface channels attached to disk drives (column 2, lines 40-54, column 5, lines 1-25).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate in Muller's device Day's interface comprising a SCSI controller in order to provide for a simple, lower cost RAID

controller architecture to enable lower cost and complexity associated with high performance and high reliability storage subsystems.

As per claim 5, Muller discloses the network interface device of claim 1.
Muller does not explicitly disclose the interface further comprising a RAID controller connectable to the storage unit.
However, Day discloses a RAID controller that integrates onto a single integrated circuit of a general-purpose processor (column 2, lines 11-25, 55-67).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate in Muller's device Day's interface comprising a RAID controller allowing the disk interface connections and protocols to be more flexibly selected but at the cost of less integration within the circuit.

As per claim 14, Muller discloses the interface device of claim 8.
Muller does not explicitly disclose the interface device comprising a SCSI controller adapted to connect with the storage unit.
However, Day discloses SCSI interface channels attached to disk drives (column 2, lines 40-54, column 5, lines 1-25).

Therefore, one of ordinary skill in the art at the time the invention was made would have found it obvious to implement or incorporate in Muller's device Day's interface comprising a SCSI controller in order to provide for a simple, lower cost RAID

controller architecture to enable lower cost and complexity associated with high performance and high reliability storage subsystems.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barbara N Burgess whose telephone number is (571) 272-3996. The examiner can normally be reached on M-F (8:00am-4:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571) 272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barbara N Burgess
Examiner
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